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09/823,700	03/30/2001	Philippe Molson	ALTRP058/A590	7449

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BEYER WEAVER & THOMAS LLP
P.O. BOX 778
BERKELEY, CA 94704-0778

EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,700	MOLSON ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-60 of the application have been examined.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statements filed on March 28, 2001 together with copies of the patents and papers. The patents and papers have been considered.

Drawings

3. The drawings submitted on March 30, 2001 are accepted.

Specification

4. The disclosure is objected to because of the following informalities:

Page 17, Lines 18-20, "This are about 47 logic elements, approximately 0.3% of the area of a typical PLD" appears to be incorrect and it appears that it should be "There are about 47 logic elements, covering approximately 0.3% of the area of a typical PLD".

Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 34-53 are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

Independent claim 34 recites a computer program product for controlling use of hardware and software. The limitations recited in claim contain computer code for executing various steps and a computer readable medium that stores the computer codes which are not statutory subject matter. To be statutory, the computer program product should include computer executable instructions which when executed in a computer performs a process comprising the steps included in the limitations.

Dependent claims 35-53 recite a computer program product. The limitations recited in claim contain the features implemented in the computer program which are not statutory subject matter. To be statutory, the computer program product should include computer executable instructions which when executed in a computer performs a process comprising the steps included in the dependent claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1, 34 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507).

9.1 **Riley et al.** teaches Data processing method and system. Specifically, as per claim 1, **Riley et al.** teaches a method for controlling use of hardware and software (Abstract, L1-23); the method comprising:

identifying a production operation range (CL4, L15-31).

Riley et al. does not expressly teach identifying a parameter having a prototype operation range wherein a portion the prototype operation range is outside of the production operation range. **Uchida et al.** teaches identifying a parameter having a prototype operation range wherein a portion the prototype operation range is outside of the production operation range (CL10, L14-32; Fig. 1), because the particular set of parameter values of the prototype corresponding to the particular composing elements minimizes the potential energy and results in optimum set of parameter values (CL116, L58-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Uchida et al.** that included identifying a parameter having a prototype operation range wherein a portion the prototype operation range is outside of the production operation range. The artisan would have been motivated because the particular set of parameter values of the prototype corresponding to the particular composing elements would minimize the potential energy and result in optimum set of parameter values.

Riley et al. does not expressly teach limiting operation of the hardware and software to the portion of the prototype operation range outside of the production operation range. **Coyle et al.** teaches limiting operation of the hardware and software to the portion of the prototype operation range outside of the production operation range (CL32, L66 to CL 33, L12; CL33, L55 to CL34, L15; Fig. 1), because that would allow operational testing to confirm and validate the calculated specifications, and verify the simulation models and results (CL33, L6-8). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Coyle et al.** that included limiting operation of the hardware and software to the portion of the prototype operation range outside of

the production operation range. The artisan would have been motivated because the particular set of parameter values of the prototype corresponding to the particular composing elements would minimize the potential energy and result in optimum set of parameter values.

9.2 As per Claim 34, it is rejected based on the same reasoning as Claim 1, supra. Claim 34 is a computer program product claim reciting the same limitations as Claim 1, as taught throughout by **Riley et al., Uchida et al.** and **Coyle et al.**

9.3 As per claim 54, **Riley et al.** teaches a method for enabling controlled operation of hardware (Abstract, L1-23).

Riley et al. does not expressly teach identifying an operational parameter having a first operation range and a second operation range, wherein a portion of the first operation range is outside of the second operation range. **Uchida et al.** teaches identifying an operational parameter having a first operation range and a second operation range, wherein a portion of the first operation range is outside of the second operation range (CL10, L14-32; Fig. 1), because the particular set of parameter values corresponding to the particular composing elements minimizes the potential energy and results in optimum set of parameter values (CL116, L58-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Uchida et al.** that included identifying an operational parameter having a first operation range and a second operation range, wherein a portion of the first operation range is outside of the second operation range. The artisan would have been motivated because the particular set of parameter values corresponding to the

particular composing elements would minimize the potential energy and result in optimum set of parameter values.

Riley et al. does not expressly teach limiting operation of the hardware to the portion of the first operation range outside of the second operation range. **Coyle et al.** teaches limiting operation of the hardware to the portion of the first operation range outside of the second operation range (CL32, L66 to CL 33, L12; CL33, L55 to CL34, L15; Fig. 1), because that would allow operational testing to confirm and validate the calculated specifications, and verify the simulation models and results (CL33, L6-8). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Coyle et al.** that included limiting operation of the hardware to the portion of the first operation range outside of the second operation range. The artisan would have been motivated because the particular set of parameter values of the prototype corresponding to the particular composing elements would minimize the potential energy and result in optimum set of parameter values.

10. Claims 2, 3, 19, 20, 35, 51, 52, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507) and **Gardner et al.** (U.S. Patent 6,346,427).

10.1 As per claims 2 and 3, **Riley et al., Uchida et al.** and **Coyle et al.** teach the method of claim 1. **Riley et al.** does not expressly teach that the prototype operation range and production

operation range overlap; and the parameter is a hardware parameter. **Gardner et al.** teaches that the prototype operation range and production operation range overlap; and the parameter is a hardware parameter (Abstract, L1-4; CL4, L36-40), because that would allow tuning the parameters of the product after the prototype verification of the gate arrays, thus decreasing the cost of the fabrication process (CL4, L36-39). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Gardner et al.** that included the prototype operation range and production operation range having overlap; and the parameter being a hardware parameter. The artisan would have been motivated because that would allow tuning the parameters of the product after the prototype verification of the gate arrays, thus decreasing the cost of the fabrication process.

10.2 As per claim 19, **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** teach the method of claim 2. **Riley et al.** does not expressly teach that the step of identifying a parameter comprises the step of identifying multiple parameters in accordance with the identification step and further wherein the step of limiting operation of the hardware and software comprises the step of limiting operation of the hardware and software with regard to each identified parameter in accordance with the limitation step. **Gardner et al.** teaches that the step of identifying a parameter comprises the step of identifying multiple parameters in accordance with the identification step and further wherein the step of limiting operation of the hardware and software comprises the step of limiting operation of the hardware and software with regard to each identified parameter in accordance with the limitation step (Abstract, L1-4; CL4, L36-40), because that would allow tuning the parameters of the product after the prototype verification of

the gate arrays (CL4, L36-39). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Gardner et al.** that included the step of identifying a parameter comprising the step of identifying multiple parameters in accordance with the identification step and further wherein the step of limiting operation of the hardware and software comprising the step of limiting operation of the hardware and software with regard to each identified parameter in accordance with the limitation step. The artisan would have been motivated because that would allow tuning the parameters of the product after the prototype verification of the gate arrays.

10.3 As per claim 20, **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** teach the method of claim 2. **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** also teach hardware device implementing the method of Claim 2, as presented in Paragraph 8.1 above.

10.4 As per Claim 35, it is rejected based on the same reasoning as Claim 2, supra. Claim 35 is a computer program product claim reciting the same limitations as Claim 2, as taught throughout by **Riley et al., Uchida et al. Coyle et al.** and **Gardner et al.**

10.5 As per Claim 51, it is rejected based on the same reasoning as Claim 19, supra. Claim 51 is a computer program product claim reciting the same limitations as Claim 19, as taught throughout by **Riley et al., Uchida et al. Coyle et al.** and **Gardner et al**

10.6 As per Claim 52, it is rejected based on the same reasoning as Claim 20, supra. Claim 52 is a computer program product claim reciting the same limitations as Claim 20, as taught throughout by **Riley et al., Uchida et al. Coyle et al.** and **Gardner et al**

10.7 As per claims 55 and 56, **Riley et al., Uchida et al.** and **Coyle et al.** teach the method of claim 54. **Riley et al.** does not expressly teach that the first operation range and the second operation range overlap; and the first operation range and the second operation range are mutually exclusive. **Gardner et al.** teaches that the first operation range and the second operation range overlap; and the first operation range and the second operation range are mutually exclusive (Abstract, L1-4; CL4, L36-40), because that would allow tuning the parameters of the product after the prototype verification of the gate arrays, thus decreasing the cost of the fabrication process (CL4, L36-39). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Gardner et al.** that included the first operation range and the second operation range overlapping; and the first operation range and the second operation range would be mutually exclusive. The artisan would have been motivated because that would allow tuning the parameters of the product after the prototype verification of the gate arrays, thus decreasing the cost of the fabrication process.

11. Claims 4 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view

of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427) and **Hurvig et al.** (U.S. Patent 6,507,592).

11.1 As per claim 4, **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** teach the method of claim 3. **Riley et al.** does not expressly teach that the hardware parameter is a data format. **Hurvig et al.** teaches that the hardware parameter is a data format (CL14, L3-5), because the circuitry may be specific to the data format (CL14, L3-5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Hurvig et al.** that included the hardware parameter being a data format. The artisan would have been motivated because the circuitry might be specific to the data format.

11.2 As per Claim 36, it is rejected based on the same reasoning as Claim 4, supra. Claim 36 is a computer program product claim reciting the same limitations as Claim 4, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al.** and **Hurvig et al.**

12. Claims 5-8, 21, 37-40 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427) and **Lin** (U.S. Patent 6,421,251).

12.1 As per claim 5, **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** teach the method of claim 3. **Riley et al.** does not expressly teach that the hardware parameter is the number of pin contacts between the hardware and an external device. **Lin** teaches that the hardware parameter is the number of pin contacts between the hardware and an external device (CL6, L63-64; CL29, L31-32; CL30, L7-9), because the number of pins used vary from chip to chip based on the location of the interconnections on the board (CL6, L67 to CL7, L1); and the number of pin usage is minimized (CL29, L13). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Lin** that included the hardware parameter being the number of pin contacts between the hardware and an external device. The artisan would have been motivated because the number of pins used would vary from chip to chip based on the location of the interconnections on the board; and the number of pin usage would be minimized.

12.2 As per claims 6-8, **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** teach the method of claim 3. **Riley et al.** does not expressly teach that the hardware parameter is a signal limit; the signal limit is a limit on the number of input signals allowed into the hardware by the software; and the signal limit is a limit on the number of output signals allowed out of the hardware by the software. **Lin** teaches that the hardware parameter is a signal limit; the signal limit is a limit on the number of input signals allowed into the hardware by the software; and the signal limit is a limit on the number of output signals allowed out of the hardware by the software (CL32, L1-5), because the number of signals determine the I/O capacity required and the number of signals that should be routed through longer paths than shortest paths (CL32, L1-

5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Lin** that included the hardware parameter being a signal limit; the signal limit being a limit on the number of input signals allowed into the hardware by the software; and the signal limit being a limit on the number of output signals allowed out of the hardware by the software. The artisan would have been motivated because the number of signals would determine the I/O capacity required and the number of signals that should be routed through longer paths than shortest paths.

12.3 As per claim 21, **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** teach the hardware device of claim 20. **Riley et al.** does not expressly teach that the device is a programmable logic device. **Lin** teaches that the device is a programmable logic device (CL57, L28-35), because the programmable logic devices contain embedded array blocks and logic array blocks which can be used to implement various memory and complex logic functions (CL57, L36-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the hardware device of **Riley et al.** with the hardware device of **Lin** that included the device being a programmable logic device. The artisan would have been motivated because the programmable logic devices would contain embedded array blocks and logic array blocks which could be used to implement various memory and complex logic functions.

12.4 As per Claims 37-40, these are rejected based on the same reasoning as Claim 5-8, supra. Claims 37-40 are computer program product claims reciting the same limitations as Claim 4, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al.** and **Lin.**

12.5 As per claim 53, **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** teach the hardware device of claim 52. **Riley et al.** does not expressly teach that the device is a programmable logic device. **Lin** teaches that the device is a programmable logic device (CL57, L28-35), because the programmable logic devices contain embedded array blocks and logic array blocks which can be used to implement various memory and complex logic functions (CL57, L36-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the hardware device of **Riley et al.** with the hardware device of **Lin** that included the device being a programmable logic device. The artisan would have been motivated because the programmable logic devices would contain embedded array blocks and logic array blocks which could be used to implement various memory and complex logic functions.

13. Claims 9 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427), **Hurvig et al.** (U.S. Patent 6,507,592) and **Lin** (U.S. Patent 6,421,251).

13.1 As per claim 9, **Riley et al., Uchida et al., Coyle et al., Gardner et al.** and **Lin** teach the method of claim 8. **Riley et al.** does not expressly teach that the output signals are signals used to provide the status of either the hardware or the software. **Hurvig et al.** teaches that the output signals are signals used to provide the status of either the hardware or the software (CL14, L37-40; CL17, L48-52), because the hardware or software status signals are used to generate

interrupt to the CPU (CL14, L37-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Hurvig et al.** that included the output signals being signals used to provide the status of either the hardware or the software. The artisan would have been motivated because the hardware or software status signals would be used to generate interrupt to the CPU.

13.2 As per Claim 41, it is rejected based on the same reasoning as Claim 9, supra. Claim 41 is a computer program product claim reciting the same limitations as Claim 9, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al., Hurvig et al.** and **Lin.**

14. Claims 10 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427) and **Gee et al.** (U.S. Patent 6,317,872).

14.1 As per claim 10, **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** teach the method of claim 3. **Riley et al.** does not expressly teach that the parameter is limited by preselected fabrication of the hardware. **Gee et al.** teaches that the parameter is limited by preselected fabrication of the hardware (CL20, L25-28), because the hardware characteristics of the system are dictated by physical fabrication parameters (CL20, L25-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Gee et al.** that included the parameter being limited by

preselected fabrication of the hardware. The artisan would have been motivated because the hardware characteristics of the system would be dictated by physical fabrication parameters.

14.2 As per Claim 42, it is rejected based on the same reasoning as Claim 10, supra. Claim 42 is a computer program product claim reciting the same limitations as Claim 10, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al.** and **Gee et al.**

15. Claims 11 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427) and **Walker** (U.S. Patent 6,157,317).

15.1 As per claim 11, **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** teach the method of claim 3. **Riley et al.** does not expressly teach that the parameter is limited by preselected augmentation of the hardware. **Walker** teaches that the parameter is limited by preselected augmentation of the hardware (CL21, L4-6), because the hardware augmentation can be performed through future modular hardware changes to affect performance (CL21, L4-6). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Walker** that included the parameter being limited by preselected augmentation of the hardware. The artisan would have been motivated because the hardware augmentation could be performed through future modular hardware changes to affect performance.

15.2 As per Claim 43, it is rejected based on the same reasoning as Claim 11, supra. Claim 43 is a computer program product claim reciting the same limitations as Claim 11, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al.** and **Walker.**

16. Claims 12 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427) and **Jin** (U.S. Patent 6,658,045).

16.1 As per claim 12, **Riley et al., Uchida et al., Coyle et al.** and **Gardner et al.** teach the method of claim 2. **Riley et al.** does not expressly teach that the parameter is a software parameter. **Jin** teaches that the parameter is a software parameter (CL4, L37-47), because the parameters entering and exiting the control unit implemented by the controller may be software parameters that are exchanged with other components (CL4, L43-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Jin** that included the parameter being a software parameter. The artisan would have been motivated because the parameters entering and exiting the control unit implemented by the controller might be software parameters that would be exchanged with other components.

16.2 As per Claim 44, it is rejected based on the same reasoning as Claim 12, supra. Claim 44 is a computer program product claim reciting the same limitations as Claim 12, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al.** and **Jin.**

17. Claims 13 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427), **Jin** (U.S. Patent 6,658,045) and **Winkelman** (U.S. Patent 4,435,752).

17.1 As per claim 13, **Riley et al., Uchida et al., Coyle et al., Gardner et al.** and **Jin** teach the method of claim 12. **Riley et al.** does not expressly teach that the parameter is a time limit on run time during which the software will permit operation of the hardware. **Winkelman** teaches that the parameter is a time limit on run time during which the software will permit operation of the hardware (CL21, L58-65), because the software can monitor the peripheral devices through their output signals and use them to initiate appropriate processing of the device requests (CL22, L6-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Winkelman** that included the parameter being a time limit on run time during which the software would permit operation of the hardware. The artisan would have been motivated because the software could monitor the peripheral devices through their output signals and use them to initiate appropriate processing of the device requests.

17.2 As per Claim 45, it is rejected based on the same reasoning as Claim 13, supra. Claim 45 is a computer program product claim reciting the same limitations as Claim 13, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al., Jin** and **Winkelman.**

18. Claims 14 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427), **Jin** (U.S. Patent 6,658,045), **Winkelman** (U.S. Patent 4,435,752) and **Mueller et al.** (U.S. Patent Re. 31,736).

18.1 As per claim 14, **Riley et al., Uchida et al., Coyle et al., Gardner et al., Jin** and **Winkelman** teach the method of claim 13. **Riley et al.** does not expressly teach the step of disabling the hardware after the time limit has been attained. **Mueller et al.** teaches the step of disabling the hardware after the time limit has been attained (CL1, L50-52), because that allows a timer or score counting circuit to disable the hardware operation after a preset time limit or number of points scored (CL1, L50-52). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Mueller et al.** that included the step of disabling the hardware after the time limit has been attained. The artisan would have been motivated because that would allow a timer or score counting circuit to disable the hardware operation after a preset time limit or number of points scored.

18.2 As per Claim 46, it is rejected based on the same reasoning as Claim 14, supra. Claim 46 is a computer program product claim reciting the same limitations as Claim 14, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al., Jin, Winkelman** and **Mueller et al.**

19. Claims 15 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427), **Jin** (U.S. Patent 6,658,045), **Winkelman** (U.S. Patent 4,435,752) **Mueller et al.** (U.S. Patent Re. 31,736) and **Lin** (U.S. Patent 6,421,251).

19.1 As per claim 15, **Riley et al., Uchida et al., Coyle et al., Gardner et al., Jin, Winkelman** and **Mueller et al.** teach the method of claim 14. **Riley et al.** does not expressly teach that the step of disabling the hardware comprises a reset of a register in the hardware. **Lin** teaches that the step of disabling the hardware comprises a reset of a register in the hardware (CL55, L11-14; CL55, L55-57), because that ensures that the output signals are logic "0" thus removing the enable signal from the hardware register model (CL55, L11-14; CL55, L55-57). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Lin** that included the step of disabling the hardware comprising a reset of a register in the hardware. The artisan would have been motivated because that would ensure that the output signals were logic "0" thus removing the enable signal from the hardware register model.

19.2 As per Claim 47, it is rejected based on the same reasoning as Claim 15, supra. Claim 47 is a computer program product claim reciting the same limitations as Claim 15, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al., Jin, Winkelman, Mueller et al.** and **Lin.**

20. Claims 16 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427), **Jin** (U.S. Patent 6,658,045), **Winkelman** (U.S. Patent 4,435,752) **Mueller et al.** (U.S. Patent Re. 31,736) and **Ngai et al.** (U.S. Patent 6,480,027).

20.1 As per claim 16, **Riley et al., Uchida et al., Coyle et al., Gardner et al., Jin, Winkelman** and **Mueller et al.** teach the method of claim 14. **Riley et al.** does not expressly teach that disabling the hardware comprises a global tri-state of the hardware IO. **Ngai et al.** teaches that disabling the hardware comprises a global tri-state of the hardware IO (CL7, L26-35), because that allows selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa (CL7, L28-32). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Ngai et al.** that included disabling the hardware comprising a global tri-state of the hardware IO. The artisan would have been motivated because

that would allow selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa.

20.2 As per Claim 48, it is rejected based on the same reasoning as Claim 16, supra. Claim 48 is a computer program product claim reciting the same limitations as Claim 16, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al., Jin, Winkelman, Mueller et al.** and **Ngai et al.**

21. Claims 17 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427), **Jin** (U.S. Patent 6,658,045), **Winkelman** (U.S. Patent 4,435,752) **Mueller et al.** (U.S. Patent Re. 31,736) and **Watson et al.** (U.S. Patent 5,982,683).

21.1 As per claim 17, **Riley et al., Uchida et al., Coyle et al., Gardner et al., Jin, Winkelman** and **Mueller et al.** teach the method of claim 14. **Riley et al.** does not expressly teach that disabling the hardware comprises a random failure of the hardware. **Watson et al.** teaches that disabling the hardware comprises a random failure of the hardware (CL6, L20-24), because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products (CL6, L20-24). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Watson et al.** that included disabling the

hardware comprising a random failure of the hardware. The artisan would have been motivated because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products.

21.2 As per Claim 49, it is rejected based on the same reasoning as Claim 17, supra. Claim 49 is a computer program product claim reciting the same limitations as Claim 17, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al., Jin, Winkelman, Mueller et al.** and **Watson et al.**

22. Claims 18 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Gardner et al.** (U.S. Patent 6,346,427), **Jin** (U.S. Patent 6,658,045), **Winkelman** (U.S. Patent 4,435,752) **Mueller et al.** (U.S. Patent Re. 31,736), **Lin** (U.S. Patent 6,421,251) and **DeRoo et al.** (U.S. Patent 5,802,376).

22.1 As per claim 18, **Riley et al., Uchida et al., Coyle et al., Gardner et al., Jin, Winkelman** and **Mueller et al.** teach the method of claim 14. **Riley et al.** does not expressly teach that an internal clock of the hardware is used to measure the run time of the hardware. **Lin** teaches that an internal clock of the hardware is used (CL48, L3-4; CL49, L7-9), because that reduces the number of software clocks required in the system (CL49, L7-9). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Lin** that included an internal clock of the hardware

being used. The artisan would have been motivated because that would reduce the number of software clocks required in the system.

Riley et al. does not expressly teach that an internal clock of the hardware is used to measure the run time of the hardware. **DeRoo et al.** teaches that an internal clock of the hardware is used to measure the run time of the hardware (CL73, L65 to CL74, L6), because the programmable hardware timers allow predetermined time intervals to be programmed for a wide range of performance levels (CL73, L65 to CL74, L2). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **DeRoo et al.** that included an internal clock of the hardware being used to measure the run time of the hardware. The artisan would have been motivated because the programmable hardware timers would allow predetermined time intervals to be programmed for a wide range of performance levels.

22.2 As per Claim 50, it is rejected based on the same reasoning as Claim 18, supra. Claim 50 is a computer program product claim reciting the same limitations as Claim 18, as taught throughout by **Riley et al., Uchida et al. Coyle et al., Gardner et al., Jin, Winkelman, Mueller et al., Lin** and **DeRoo et al.**

23. Claims 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **Mueller et al.** (U.S. Patent Re. 31,736) and **DeRoo et al.** (U.S. Patent 5,802,376).

23.1 As per claim 22, **Riley et al.** teaches a method for controlling use of hardware that uses software (Abstract, L1-23).

Riley et al. does not expressly teach identifying a run time limit that is (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner. **Winkelman** teaches identifying a run time limit that is (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner (CL21, L58-65), because that would allow using steps to force from execution certain functions when they have exceeded a given time limit (CL21, L61-63). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Winkelman** that included identifying a run time limit that was (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner. The artisan would have been motivated because that would allow using steps to force from execution certain functions when they have exceeded a given time limit.

Riley et al. does not expressly teach counting the time elapsed during operation of the hardware. **DeRoo et al.** teaches counting the time elapsed during operation of the hardware (CL73, L65 to CL74, L6), because the programmable hardware timers allow counting the time elapsed using predetermined time intervals programmed for a wide range of performance levels (CL73, L65 to CL74, L2). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **DeRoo et al.** that included counting the time elapsed during operation of the hardware. The artisan would

have been motivated because the programmable hardware timers would allow counting the time elapsed using predetermined time intervals programmed for a wide range of performance levels.

Riley et al. does not expressly teach disabling the hardware after the run time limit is reached. **Mueller et al.** teaches disabling the hardware after the run time limit is reached (CL1, L50-52), because that allows a timer or score counting circuit to disable the hardware operation after a preset time limit or number of points scored (CL1, L50-52). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Mueller et al.** that included disabling the hardware after the run time limit is reached. The artisan would have been motivated because that would allow a timer or score counting circuit to disable the hardware operation after a preset time limit or number of points scored.

23.2 As per claim 28, **Riley et al., Winkelman, Mueller et al.** and **DeRoo et al.** teach the method of claim 22. **Riley et al., Winkelman, Mueller et al.** and **DeRoo et al.** also teach hardware device implementing the method of Claim 22, as presented in Paragraph 21.1 above.

24. Claims 23, 24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **Mueller et al.** (U.S. Patent Re. 31,736), **DeRoo et al.** (U.S. Patent 5,802,376) and **Lin** (U.S. Patent 6,421,251).

24.1 As per claim 23, **Riley et al., Winkelman, Mueller et al** and **DeRoo et al.** teach the method of claim 22. **Riley et al.** does not expressly teach that the counting step is performed by an internal clock within the hardware. **Lin** teaches that the counting step is performed by an internal clock within the hardware (CL48, L3-4; CL49, L7-9), because that reduces the number of software clocks required in the system (CL49, L7-9). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Lin** that included the counting step being performed by an internal clock within the hardware. The artisan would have been motivated because that would reduce the number of software clocks required in the system.

24.2 As per claim 24, **Riley et al., Winkelman, Mueller et al** and **DeRoo et al.** teach the method of claim 22. **Riley et al.** does not expressly teach that disabling the hardware comprises a reset of a register in the hardware. **Lin** teaches that disabling the hardware comprises a reset of a register in the hardware (CL55, L11-14; CL55, L55-57), because that ensures that the output signals are logic "0" thus removing the enable signal from the hardware register model (CL55, L11-14; CL55, L55-57). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Lin** that included disabling the hardware comprising a reset of a register in the hardware. The artisan would have been motivated because that would ensure that the output signals were logic "0" thus removing the enable signal from the hardware register model.

24.3 As per claim 29, **Riley et al., Winkelman, Mueller et al** and **DeRoo et al.** teach the hardware device of claim 28. **Riley et al.** does not expressly teach that the device is a programmable logic device. **Lin** teaches that the device is a programmable logic device (CL57, L28-35), because the programmable logic devices contain embedded array blocks and logic array blocks which can be used to implement various memory and complex logic functions (CL57, L36-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Lin** that included the device being a programmable logic device. The artisan would have been motivated because the programmable logic devices would contain embedded array blocks and logic array blocks which could be used to implement various memory and complex logic functions.

25. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **Mueller et al.** (U.S. Patent Re. 31,736), **DeRoo et al.** (U.S. Patent 5,802,376) and **Ngai et al.** (U.S. Patent 6,480,027).

25.1 As per claim 25, **Riley et al., Winkelman, Mueller et al** and **DeRoo et al.** teach the method of claim 22. **Riley et al.** does not expressly teach that disabling the hardware comprises a global tri-state of the hardware IO. **Ngai et al.** teaches that disabling the hardware comprises a global tri-state of the hardware IO (CL7, L26-35), because that allows selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa (CL7, L28-32). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the method of **Riley et al.** with the method of **Ngai et al.** that included disabling the hardware comprising a global tri-state of the hardware IO. The artisan would have been motivated because that would allow selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa.

26. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **Mueller et al.** (U.S. Patent Re. 31,736), **DeRoo et al.** (U.S. Patent 5,802,376) and **Watson et al.** (U.S. Patent 5,982,683).

26.1 As per claim 26, **Riley et al., Winkelman, Mueller et al** and **DeRoo et al.** teach the method of claim 22. **Riley et al.** does not expressly teach that disabling the hardware comprises a random failure of the hardware. **Watson et al.** teaches that disabling the hardware comprises a random failure of the hardware (CL6, L20-24), because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products (CL6, L20-24). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Watson et al.** that included disabling the hardware comprising a random failure of the hardware. The artisan would have been motivated because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products.

27. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **Mueller et al.** (U.S. Patent Re. 31,736), **DeRoo et al.** (U.S. Patent 5,802,376) , **Lin** (U.S. Patent 6,421,251), **Ngai et al.** (U.S. Patent 6,480,027) and **Watson et al.** (U.S. Patent 5,982,683).

27.1 As per claim 27, **Riley et al., Winkelman, Mueller et al** and **DeRoo et al.** teach the method of claim 22. **Riley et al.** does not expressly teach that disabling is selected from a reset of a register in the hardware. **Lin** teaches that disabling is selected from a reset of a register in the hardware (CL55, L11-14; CL55, L55-57), because that ensures that the output signals are logic "0" thus removing the enable signal from the hardware register model (CL55, L11-14; CL55, L55-57). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Lin** that included disabling being selected from a reset of a register in the hardware. The artisan would have been motivated because that would ensure that the output signals were logic "0" thus removing the enable signal from the hardware register model.

Riley et al. does not expressly teach that disabling is selected from a global tri-state of the IO of the hardware. **Ngai et al.** teaches that disabling is selected from a global tri-state of the IO of the hardware (CL7, L26-35), because that allows selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa (CL7, L28-32). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Ngai et al.** that included disabling being selected from a global tri-state of the IO of the hardware. The artisan would have

been motivated because that would allow selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa.

Riley et al. does not expressly teach that disabling is selected from a random failure within the hardware. **Watson et al.** teaches that disabling is selected from a random failure within the hardware (CL6, L20-24), because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products (CL6, L20-24). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Watson et al.** that included disabling being selected from a random failure within the hardware. The artisan would have been motivated because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products.

28. Claims 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over **DeRoo et al.** (U.S. Patent 5,802,376) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **Mueller et al.** (U.S. Patent Re. 31,736).

28.1 As per claim 30, **DeRoo et al.** teaches counter in a hardware device, said counter comprising a clock and a memory containing a run time limit measured by the clock (CL73, L65 to CL74, L6).

DeRoo et al. does not expressly teach the run time limit being (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a

production manner. **Winkelman** teaches the run time limit being (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner (CL21, L58-65), because that would allow using steps to force from execution certain functions when they have exceeded a given time limit (CL21, L61-63). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the counter of **DeRoo et al.** with the counter of **Winkelman** that included the run time limit being (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner. The artisan would have been motivated because that would allow using steps to force from execution certain functions when they have exceeded a given time limit.

DeRoo et al. does not expressly teach means for disabling the hardware device after, the run time limit is reached by the clock. **Mueller et al.** teaches means for disabling the hardware device after, the run time limit is reached by the clock (CL1, L50-52), because that allows a timer or score counting circuit to disable the hardware operation after a preset time limit or number of points scored (CL1, L50-52). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the counter of **DeRoo et al.** with the counter of **Mueller et al.** that included means for disabling the hardware device after, the run time limit was reached by the clock. The artisan would have been motivated because that would allow a timer or score counting circuit to disable the hardware operation after a preset time limit or number of points scored.

28.2 As per claim 32, **DeRoo et al., Winkelman** and **Mueller et al** teach the counter of claim 30. **DeRoo et al., Winkelman** and **Mueller et al.** also teach hardware device comprising the counter of Claim 30, as presented in Paragraph 26.1 above.

29. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over **DeRoo et al.** (U.S. Patent 5,802,376) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **Mueller et al.** (U.S. Patent Re. 31,736), **Lin** (U.S. Patent 6,421,251), **Ngai et al.** (U.S. Patent 6,480,027) and **Watson et al.** (U.S. Patent 5,982,683).

29.1 As per claim 31, **DeRoo et al., Winkelman** and **Mueller et al** teach the counter of claim 30. **DeRoo et al.** does not expressly teach that disabling is selected from a reset of a register in the hardware. **Lin** teaches that disabling is selected from a reset of a register in the hardware (CL55, L11-14; CL55, L55-57), because that ensures that the output signals are logic "0" thus removing the enable signal from the hardware register model (CL55, L11-14; CL55, L55-57). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the counter of **DeRoo et al.** with the counter of **Lin** that included disabling being selected from a reset of a register in the hardware. The artisan would have been motivated because that would ensure that the output signals were logic "0" thus removing the enable signal from the hardware register model.

DeRoo et al. does not expressly teach that disabling is selected from a global tri-state of the IO of the hardware. **Ngai et al.** teaches that disabling is selected from a global tri-state of the IO of the hardware (CL7, L26-35), because that allows selectively driving signals from input

pins or input/output pins or adjacent logic regions onto conductor segments or vice versa (CL7, L28-32). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the counter of **DeRoo et al.** with the counter of **Ngai et al.** that included disabling being selected from a global tri-state of the IO of the hardware. The artisan would have been motivated because that would allow selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa.

DeRoo et al. does not expressly teach that disabling is selected from a random failure within the hardware. **Watson et al.** teaches that disabling is selected from a random failure within the hardware (CL6, L20-24), because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products (CL6, L20-24). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the counter of **DeRoo et al.** with the counter of **Watson et al.** that included disabling being selected from a random failure within the hardware. The artisan would have been motivated because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products.

30. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over **DeRoo et al.** (U.S. Patent 5,802,376) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **Mueller et al.** (U.S. Patent Re. 31,736) and **Lin** (U.S. Patent 6,421,251).

30.1 As per claim 33, **DeRoo et al., Winkelman** and **Mueller et al** teach hardware device of claim 32. **DeRoo et al.** does not expressly teach that the device is a programmable logic device. **Lin** teaches that the device is a programmable logic device (CL57, L28-35), because the programmable logic devices contain embedded array blocks and logic array blocks which can be used to implement various memory and complex logic functions (CL57, L36-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the counter of **DeRoo et al.** with the counter of **Lin** that included the device being a programmable logic device. The artisan would have been motivated because the programmable logic devices would contain embedded array blocks and logic array blocks which could be used to implement various memory and complex logic functions.

31. Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), and **Winkelman** (U.S. Patent 4,435,752).

31.1 As per claim 57, **Riley et al., Uchida et al.** and **Coyle et al.** teach the method of claim 54. **Riley et al.** does not expressly teach that the operational parameter is time. **Winkelman** teaches that the operational parameter is time (CL21, L58-65), because the software can monitor the program execution and force from execution certain functions when they have exceeded a given time limit (CL21, L61-62. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Winkelman** that included the operational parameter being time. The artisan would have been

motivated because the software could monitor the program execution and force from execution certain functions when they had exceeded a given time limit.

Riley et al. does not expressly teach that the first operation range is a prototype testing time range and the second operation range is a production time range. **Uchida et al.** teaches that the first operation range is a prototype testing time range and the second operation range is a production time range (CL10, L14-32; Fig. 1), because the particular set of parameter values of the prototype corresponding to the particular composing elements minimizes the potential energy and results in optimum set of parameter values (CL116, L58-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Uchida et al.** that included the first operation range being a prototype testing time range and the second operation range being a production time range. The artisan would have been motivated because the particular set of parameter values of the prototype corresponding to the particular composing elements would minimize the potential energy and result in optimum set of parameter values.

32. Claims 58-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Riley et al.** (U.S. Patent 6,633,788) in view of **Uchida et al.** (U.S. Patent 6,336,107), and further in view of **Coyle et al.** (U.S. Patent 6,546,507), **Winkelman** (U.S. Patent 4,435,752) and **Hurvig et al.** (U.S. Patent 6,507,592).

32.1 As per claims 58-60, **Riley et al., Uchida et al., Coyle et al.** and **Winkelman** teach the method of claim 57. **Riley et al.** does not expressly teach that the prototype testing time range

has a maximum and further wherein the production time range has no maximum; the first operation range is a range of timed operation having a maximum time limit and wherein the second operation range is a range of timed operation extending beyond the maximum time limit; and the second operation range has no maximum time limit. **Hurvig et al.** teaches that that the prototype testing time range has a maximum and further wherein the production time range has no maximum; the first operation range is a range of timed operation having a maximum time limit and wherein the second operation range is a range of timed operation extending beyond the maximum time limit; and the second operation range has no maximum time limit (CL3, L13-29; CL7, L42-45), because substantial time period is required for testing the prototypes and preparing a new product (CL3, L15-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Riley et al.** with the method of **Hurvig et al.** that included the prototype testing time range having a maximum and further wherein the production time range had no maximum; the first operation range was a range of timed operation having a maximum time limit and wherein the second operation range was a range of timed operation extending beyond the maximum time limit; and the second operation range had no maximum time limit. The artisan would have been motivated because substantial time period would be required for testing the prototypes and preparing a new product.

Conclusion

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
August 6, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER